Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte QUE-WON RHEE

Appeal No. 2004-0932
Application No. 09/432,819

ON BRIEF

Before BARRETT, BARRY, and BLANKENSHIP, *Administrative Patent Judges.*
BARRY, *Administrative Patent Judge.*

DECISION ON APPEAL

A patent examiner rejected claims 1, 2, 4, and 6-12. The appellant appeals therefrom under 35 U.S.C. § 134(a). We affirm-in-part.

BACKGROUND

The invention at issue on appeal concerns interfacing. Within an integrated circuit ("IC"), it is sometimes necessary for a port of a specialized logic block — the specialized logic block may be proprietary to a particular vendor — to interface with an on-chip bus. Accordingly, the appellant's interface block (19) provides an interface

between an internal bus (15) of an IC (200) and a socket (20 and 25) of a specialized logic block (10). The interface block comprises modules. A synchronization module (11) synchronizes the clock domain of the internal bus and the clock domain of the socket. (Spec. at 1.) A translation module (12) translates block encoding of data transferred between the internal bus and the socket. (*Id.* at 1-2.) A queue module (13) buffers data flowing between the internal bus and the socket. A driver module (14) handles low level and electrical drive specifications of the internal bus. According to the appellant, the modularity of the interface block enables rapid assembly. (*Id.* at 2.)

Each module can be customized. For example, the synchronization module can be implemented as a null synchronization block (61) where no synchronization is required between the clock domains, as a ratio synchronization block (81) where the clock domains are related by a fixed ratio, or as a full synchronization block (101) where no phase relationship exists between the clock domains. The appellant asserts that customization of the modules enables the interface block to be compatible with a variety of proprietary logic blocks and on-chip busses. (*Id.*)

A further understanding of the invention can be achieved by reading the following claims.

4. A method for providing an interface between an internal bus of an integrated circuit and a socket of a logic block within the integrated circuit, the method comprising the steps of:

(a) performing any needed synchronization between a clock domain of the internal bus and a clock domain of the socket of the logic block within a synchronization module;

(b) providing any required translation of block encoding of data transferred between the internal bus and the socket of the logic block using a translation module;

(c) buffering data flowing between the internal bus and the socket of the logic block using a queue module; and,

(d) handling low level and electrical drive specifications of the internal bus using a driver module.

7. On an integrated circuit, an interface block that provides an interface between an internal bus of the integrated circuit and a socket of a logic block, the interface block comprising:

a plurality of modules connected in series, wherein each module in the plurality of modules performs only a single function from a plurality of functions;

wherein any needed synchronization between a clock domain of the internal bus and a clock domain of the socket of the logic block is a first function from the plurality of functions, any required translation of block encoding of data is a second function from the plurality of functions, any buffering of data flowing between the internal bus and the socket of the logic block is a third function from the plurality of functions, and

handling any low level and electrical drive specifications of the internal bus is a fourth function from the plurality of functions.

Claims 1, 2, 4, and 6-12 stand rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 5,870,310 ("Malladi").

OPINION

Our opinion addresses the claims in the following order:

- claims 1, 2, 4, and 6
- claims 7-12.

A. CLAIMS 1, 2, 4, AND 6

Rather than reiterate the positions of the examiner or the appellant *in toto*, we focus on the main point of contention therebetween. The examiner asserts, "Malladi teaches, for example, a synchronization module [e.g., MIU 150a] and a driver [BIU 140a] are within the same interface block [shell 141a] and interface to the same bus [CPU bus 100]. . . ." (Examiner's Answer at 9.) The appellant argues, "[w]hile MIU 150b and BIU 140b are both within shell 141b, they clearly do not interface to the same bus." (Reply Br. at 5.)

"[T]here is no anticipation 'unless all of the same elements are found in exactly the same situation and united in the same way . . . in a single prior art reference.'" *Perkin-Elmer Corp. v. Computervision Corp.*, 732 F.2d 888, 894, 221 USPQ 669, 673 (Fed. Cir. 1984) (citing *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 771, 218 USPQ 781, 789 (Fed. Cir. 1983). "[A]bsence from the reference of any claimed element negates anticipation." *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Here, Malladi "us[es] IC shells having reusable interface logic suitable to provide appropriate interfacing between a multiplicity of integrated circuit cores and buses. The IC shells are preferably designed for one application, stored in an IC shell library, and reused in future applications with little or no time consumed in their redesign, characterization, and testing." Col. 3, ll. 31-38. Figure 1 of the reference "illustrates an integrated circuit design labeled as 'Application-1.' By way of example, Application-1 may be a system-on-a-chip design for digital audio/video decoder." *Id.* at ll. 39-41.

"Application-1 (of FIG. 1) . . . shows three data processing shells 141a, 141b, 141c having three data processing cores 108, 110, and 112 respectively. Each of the three shells has a number of interfacing logic cells selected to aid the proper reception,

transmission and processing of data in and out of the respective shells." Col. 4, ll. 60-65. "[D]ata processing shells 141a-141c have associated bus interface units (BIUs) 140a-140c . . . , and memory interface units (MIUs) 150a-150c. . . ." Col. 4, l. 65 - col. 5, l. 1. BIU 140a and MIU 150a do not, however, "interface to the same bus [CPU bus 100]. . . ." (Examiner's Answer at 9.) To the contrary, although BIU 140a (as well as BIUs 140b and 140c) "interface[s] with CPU bus 100," col. 4, l. 67 - col. 5, l. 1, MIU 150a (as well as MIUs 150 and 150b) "interface[s] with memory bus 102." Col. 5, l. 2. Therefore, we reverse the anticipation rejection of claims 1, 2, 4, and 6.

B. CLAIMS 7-12

"[T]o assure separate review by the Board of individual claims within each group of claims subject to a common ground of rejection, an appellant's brief to the Board must contain a clear statement for each rejection: (a) asserting that the patentability of claims within the group of claims subject to this rejection do not stand or fall together, and (b) identifying which individual claim or claims within the group are separately patentable and the reasons why the examiner's rejection should not be sustained." *In re McDaniel*, 293 F.3d 1379, 1383, 63 USPQ2d 1462, 1465 (Fed. Cir. 2002) (citing 37 C.F.R. §1.192(c)(7) (2001)). "If the brief fails to meet either requirement, the Board is free to select a single claim from each group of claims subject to a common ground of

rejection as representative of all claims in that group and to decide the appeal of that rejection based solely on the selected representative claim." *Id.*, 63 USPQ2d at 1465.

Here, the appellant groups "claims 7 through 12," (Appeal Br. at 4.) The only claim from the group that he argues separately is claim 7. (*Id.* at 13-14.) Therefore, we select claim 7 from the group as representative of the claims therein. With this representation in mind, we focus on the two points of contention between the examiner and the appellant, which follow:

- modules
- functions.

1. Modules

The examiner finds, "Malladi teaches an interface block that comprises a plurality of modules [e.g., logic cells 140a, 108, 150a inside of shell 141a, logic cells 140b, 110, 150b inside of shell 141b, logic cells 240b, 110, 250b inside of shell 141b', logic cells 302, 304, 308 inside of shell 301, logic cells 302, 306, 312 inside of shell 301, logic cells 310, 306, 312 inside of shell 301, logic cells 336, 328, 332, 334, 326 inside of shell 327, logic cells 340, 342, 344, 346 inside of shell 337, or logic cells 340, 338, 336 inside of shell 337] connected in series." (Examiner's Answer at 10-11.) The appellant argues, "nowhere in Malladi is there disclosed an interface block that

comprises a plurality of modules. Nowhere in Malladi is there disclosed a plurality of modules connected in series." (Appeal Br. at 13.)

In addressing the point of contention, the Board conducts a two-step analysis. First, we construe the representative claim at issue to determine its scope. Second, we determine whether the construed claim is anticipated.

a. Claim Construction

"Analysis begins with a key legal question — *what* is the invention *claimed*?" *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). In answering the question, "the Board must give claims their broadest reasonable construction. . . ." *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1668 (Fed. Cir. 2000). "Moreover, limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993) (citing *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)).

Here, claim 7 recites in pertinent part the following limitations: "the interface block comprising: a plurality of modules connected in series. . . ." Giving the

representative claim its broadest, reasonable construction, the limitations require an interface comprising serially-connected components.

b. Anticipation Determination

"Having construed the claim limitations at issue, we now compare the claims to the prior art to determine if the prior art anticipates those claims." *In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349, 64 USPQ2d 1202, 1206 (Fed. Cir. 2002). "[A]nticipation is a question of fact." *Hyatt*, 211 F.3d at 1371, 54 USPQ2d at 1667 (citing *Bischoff v. Wethered*, 76 U.S. (9 Wall.) 812, 814-15 (1869); *In re Schreiber*, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997)). "A claim is anticipated . . . if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) (citing *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 715, 223 USPQ 1264, 1270 (Fed. Cir. 1984); *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548, 220 USPQ 193, 198 (Fed. Cir. 1983); *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 771, 218 USPQ 781, 789 (Fed. Cir. 1983)). Of course, "this is not an 'ipsissimis verbis' test." *In re Bond*, 910 F.2d 831, 832, 15 USPQ2d 1566, 1567 (Fed. Cir. 1990) (citing *Akzo N.V.*

v. United States Int'l Trade Comm'n, 808 F.2d 1471, 1479 & n.11, 1 USPQ2d 1241, 1245 & n.11 (Fed. Cir. 1986)).

Here, Figure 3 of Malladi shows "the interface logic shells used to decode video and audio data. . . ." Col. 3, ll. 24-25. "[F]our interface shells are provided: a CPU shell 317, a stream interface shell 301, a video shell 327, and an audio shell 337. Each of these shells houses one or more data processing cores, dedicated to specific data processing tasks. In addition, the shells contain various interface logic cells to support the main data processing cores." Col. 6, ll. 23-29. Figure 3 shows that the stream interface shell 301 comprises serially-connected components such as "a memory interface unit (MIU) 312," Col. 7, l. 11; "a hardware block 302 where a byte alignment operation is performed," Col. 6, ll. 42-43; "a buffer block 306," *id.* at l. 54; and a BIU 310.

2. Functions

Asserting that "claim 7 sets out that each module in the plurality of modules performs only a single function from a plurality of functions," (Reply Br. at 7), the appellant argues,"[i]n *Malladi*, there is no such division of functions among, for example, between BIU 140a, data processing core 108, and MIU 150a or between BIU 140b, data processing core 110, and MIU 150b." (*Id.* at 8.)

a. Claim Construction

Claim 7 further recites in pertinent part the following limitations: "each module in the plurality of modules performs only a single function from a plurality of functions. . . ." Giving the representative claim its broadest, reasonable construction, the limitations require that each of the aforementioned components performs only one of the following four functions: synchronization, translation, buffering, and handling any low level and electrical drive specifications. The claim does no preclude the components from performing any additional functions besides the aforementioned four.

b. Anticipation Determination

The examiner finds that Malladi's MIU 312 "performs any needed synchronization [timing requirements in col. 2, lines 3-9] between a clock domain [e.g., various clock of Pentium, PowerPC, SPARC, or MIPS processor in col. 3, lines 42-48] of the internal bus and a clock domain [e.g., various clock of ISA, AT ISA, PCI, EISA, or MCA bus in col. 4, lines 43-56] of the socket of the logic block. . . ." (Examiner's Answer at 3.) The reference supports this finding by disclosing that "[a]s is well known in the art, MIU's are generally selected to provide proper interfacing between functional cores and buses." Col. 4, ll. 38-40. Because a "bit stream will be processed in a hardware block 302 where a byte alignment operation is performed," col. 6, ll. 42-43.

"to align the serial bit stream into parallel byte (i.e., 8 bits) size units," *id.* at ll. 43-45, we find that Malladi's byte alignment block 302 performs translation.

Because "the payload associated with the video bit stream is temporarily stored in a buffer block 306," *id.* at ll. 52-54, we further find that the reference's buffer 306 performs buffering. The examiner further finds that Malladi's BIU 310 "handles [col. 4, lines 62-65 and col. 4, lines 35-38] low level and electrical drive specifications of the internal bus." (Examiner's Answer at 4.) The reference supports this finding by disclosing that BIUs "establish appropriate communications protocols with CPU bus. . . ." Col. 3, ll. 58-59.

In summary, Malladi's MIU, byte alignment block, buffer, and BIU each perform one of the following four functions: synchronization, translation, buffering, and handling any low level and electrical drive specifications. Any additional functions outside the aforementioned four that might be performed by one of more of these components are not precluded by the claim. Therefore, we affirm the anticipation rejection of claim 7 and of claims 8-12, which fall therewith.

CONCLUSION

In summary, the rejection of claims 1, 2, 4, and 6 under § 102(e) is reversed. The rejection of claims 7-12 under § 102(e), however, is affirmed.

"Any arguments or authorities not included in the brief will be refused consideration by the Board of Patent Appeals and Interferences. . . ." 37 C.F.R. § 1.192(a). Accordingly, our affirmance is based only on the arguments made in the briefs. Any arguments or authorities omitted therefrom are neither before us nor at issue but are considered waived. *Cf. In re Watts*, 354 F.3d 1362, 1367, 69 USPQ2d 1453, 1457 (Fed. Cir. 2004) ("[I]t is important that the applicant challenging a decision not be permitted to raise arguments on appeal that were not presented to the Board.") No time for taking any action connected with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

LEE E. BARRETT
Administrative Patent Judge

LANCE LEONARD BARRY
Administrative Patent Judge

HOWARD B. BLANKENSHIP
Administrative Patent Judge

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